IN THE CLAIMS

Please amend the claims as follows:

1-17. (Previously Canceled)

18. (Currently Amended) A method comprising:

forming at least one first trench within a semiconductor substrate at a first depth;

depositing a first conductive material, which has a melting point high enough to prevent unwanted metallurgical changes during subsequent processing, substantially at the bottom of each first trench;

forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth;

depositing a second conductive material, which has a melting point high enough to prevent unwanted metallurgical changes during subsequent processing, substantially at the bottom of each second trench; ~~and~~

surrounding the first conductive material and the second conductive material with an insulative material to prevent short circuiting between the first conductive material and the second conductive material and to provide electrical insulation between the first and second conductive materials and the semiconductor substrate; and

connecting the first conductive material to conductive parts that extend upwardly on opposite sides of the second conductive material beyond the second depth.

19. (Original) The method of claim 18, wherein the first conductive material is identical to the second conductive material.

20. (Original) The method of claim 18, wherein at least one of the first conductive material and the second conductive material comprises one of tungsten and a tungsten alloy.

21. (Previously Amended) The method of claim 18, further comprising between forming at least one first trench and depositing a first conductive material, depositing a seed material to facilitate deposition of the first conductive material.

22. (Original) The method of claim 21, wherein the seed material comprises titanium.

23. (Original) The method of claim 21, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

24. (Previously Amended) The method of claim 18, further comprising between forming at least one second trench and depositing a second conductive material, depositing a seed material to facilitate deposition of the second conductive material.

25. (Original) The method of claim 24, wherein the seed material comprises titanium.

26. (Original) The method of claim 24, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

27. (Previously Amended) The method of claim 18, further comprising between depositing a first conductive material and forming at least one second trench, depositing the insulative material within each first trench over the first conductive material.

28. (Original) The method of claim 27, wherein the insulative material comprises silicon dioxide.

29. (Previously Amended) The method of claim 18, further comprising after depositing a second conductive material, depositing a further insulative material within each second trench over the second conductive material.

30. (Previously Amended) The method of claim 29, wherein the further insulative material comprises silicon dioxide.

31. (Previously Amended) The method of claim 18, further comprising between forming at least one first trench and depositing a first conductive material, forming the insulating layer at the bottom of and on walls of each first trench.

32. (Original) The method of claim 31, wherein forming the insulating layer comprises oxidizing the bottom of and the walls of each first trench.

33. (Previously Amended) The method of claim 18, further comprising between forming at least one second trench and depositing a second conductive material, forming a second insulating layer at the bottom of and on walls of each second trench.

34. (Previously Amended) The method of claim 33, wherein forming the second insulating layer comprises oxidizing the bottom of and the walls of each second trench.

35. (Original) The method of claim 18, wherein at least one of the first conductive material and the second conductive material is deposited by a selective deposition process.

36. (Original) The method of claim 35, wherein the selective deposition process is selected from the group essentially consisting of chemical vapor deposition and plating.

37. (Previously Amended) The method of claim 18, wherein the semiconductor substrate is part of a wafer having a front side and a back side, and further comprising after depositing a second conductive material, thinning the back side of the wafer to expose at least one of the first conductive material and the second conductive material.

38. (Previously Amended) The method of claim 18, further comprising after depositing a second conductive material, connecting at least one of the first conductive material with at least one of the second conductive material.

39. (Currently Amended) A method comprising:

burying first conductive elements within a semiconductor substrate at a first depth;

burying second conductive elements within a semiconductor substrate at a second depth less than the first depth;

connecting the first conductive elements to conductive parts that extend upwardly on opposite sides of the second conductive elements beyond the second depth; and

surrounding the first conductive elements and the second conductive elements to prevent short circuiting and to electrically insulate the first and second conductive elements from the semiconductor substrate.

40. (Original) The method of claim 39, wherein the first conductive elements and the second conductive elements each comprise a predetermined material.

41. (Original) The method of claim 39, wherein each of burying first conductive elements and burying second conductive elements comprises:

forming at least one trench within a semiconductor substrate, each trench having walls and a bottom;

forming an insulating layer at the bottom and on the walls of the trench;

depositing a seed material at the bottom of each trench;

depositing a conductive material within each trench over the seed material; and,

depositing an insulative material within each trench over the conductive material.

42. (Currently Amended) A method, comprising:

forming communication layers in a substrate;

forming an active semiconductor layer above the communication layers on the substrate; and

wherein forming the communication layers includes:

forming at least one first trench within a semiconductor substrate at a first depth;

forming a first insulating layer at a bottom and sidewalls of the at least one first trench;

depositing a first seed material to facilitate deposition of a first conductive material in the at least one first trench;

depositing the first conductive material substantially at the bottom of each first trench;

forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth;

forming a second insulating layer at a bottom and sidewalls of the at least one second trench;

depositing a second seed material to facilitate deposition of a second conductive material in the at least one second trench;

depositing the second conductive material substantially at the bottom of each second trench;

forming a third insulating layer on the first conductive material to prevent short circuiting to the second conductive material; ~~and~~

electrically insulating the first conductive layer from the semiconductor substrate; and

connecting the first conductive material to conductive parts that extend upwardly on opposite sides of the second conductive material beyond the second depth.

43. (Previously Amended) The method of claim 42, wherein depositing the second conductive material includes forming a fourth insulating layer on the second conductive material.

44. (Previously Amended) The method of claim 43, wherein forming the active semiconductor layer includes forming the active semiconductor layer on the fourth insulating layer.

45. (Previously Amended) The method of claim 44, wherein forming the active semiconductor layer includes forming a P-type epitaxial layer on the fourth insulating layer.

46. (Previously Added) The method of claim 45, wherein forming the active semiconductor layer includes forming an active circuitry of a semiconductor structure in the P-type epitaxial layer.

47. (Previously Amended) The method of claim 46, wherein forming the active circuitry includes forming a trench capacitor that extends between the second conductive material in two of the at least one second trenches.

48. (Previously Added) The method of claim 47, wherein forming the trench capacitor includes forming the trench capacitor with at least one first trench on opposite sides of the trench capacitor.

49. (Previously Added) The method of claim 44, wherein forming the communication layers in the substrate includes thinning the back side of the substrate to expose at least one of the first conductive material and the second conductive material.

50. (New) The method of claim 40, wherein the predetermined material has a high melting point that is adapted to prevent unwanted metallurgical changes during subsequent processing.

51. (New) A semiconductor structure comprising:

forming an active semiconductor layer on a substrate layer;

forming a first buried layer buried at a first depth within the substrate and including a plurality of substantially parallel first conductive elements oriented in a first direction and parallel to the active semiconductor layer;

forming a second buried layer buried at a second depth within the substrate and including of a plurality of substantially parallel second conductive elements oriented in a second direction orthogonal to the first direction and parallel to the active semiconductor layer, wherein forming the second buried layer includes forming the second depth greater than the first depth;

arranging insulating material to separate the first and second conductive elements,

wherein forming the first buried layer includes depositing a material with a high melting point that prevents unwanted metallurgical changes when processing the active semiconductor layer;

wherein forming the second buried layer includes depositing a material with a high melting point that prevents unwanted metallurgical changes when processing the active semiconductor layer; and

connecting the plurality of substantially parallel second conductive elements to conductive parts that extend upwardly on opposite sides of the first buried layer beyond the first depth adjacent outer ones of the plurality of substantially parallel first conductive elements.